

NICAM 728 Television Stereo Sound

Single Chip

Demultiplexer - CF70123

3Q/88



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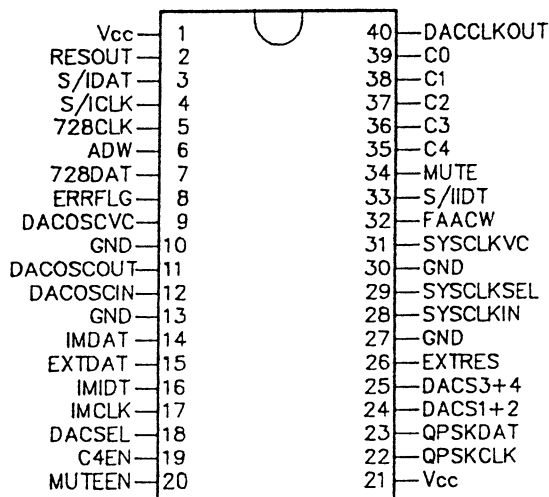


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- * Single chip solution all memory on chip.
- * Descrambles and de-Interleaves NICAM 728 Data Stream.
- * Recovers 14-bit sound samples from 10-bit companded samples.
- * User selectable D-to-A's - Philips or ITT
- * Information/control via external pins or I.M. bus interface.
- * Facility to add external pseudo random sequence generator.
- * Automatic reformatting - stereo, mono or dual language.
- * Auto muting - greater than 1 in 100 parity errors
- * Three-state Outputs to the D-to-A Converters

DUAL-IN-LINE PIN OUT



- * Compatible with full EBU NICAM specification (SPB424)

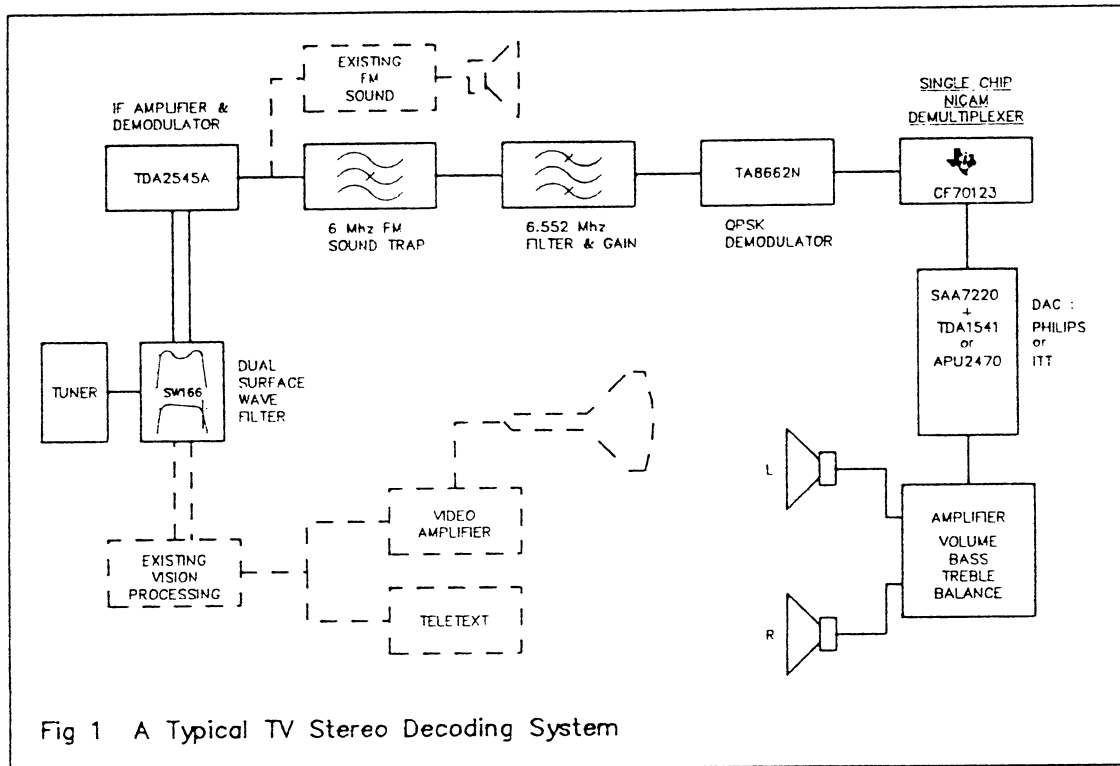
1. Description

The Texas Instruments Digital Stereo Demultiplexer takes as input a NICAM 728 encoded digital data stream. It then descrambles, deinterleaves and reformats this, to provide output to industry standard digital to analogue converters. The device also provides information about the data stream, and allows language selection in the event of a dual language transmission. An Intermetall Bus Interface is provided to allow for optional microprocessor control of the demultiplexer, and also a choice of either S-Bus or I²S-Bus format for output to the digital to analogue converters. Also available is the complete NICAM encoded data stream after it has been descrambled.

2. Application

The main application for the Stereo Demultiplexer is for use in TV Stereo Sound decoding. A typical decoding system showing where the demultiplexer fits is outlined in Figure 1. Possible future applications include, demultiplexing encrypted transmissions, and datacast applications where the demultiplexer will act as a descrambler.

**SINGLE CHIP NICAM 728
STEREO DEMULTIPLEXER
CF70123**



The decoding system consists of:-

- (i) Dual Surface Wave Filter - Plessey SW166.
- (ii) IF Amplifier and demodulator - Philips TDA2545A.
- (iii) 6.0 MHz FM Sound Trap - Twin-T Notch Filter.
At least 30 dB's attenuation at 6.0 MHz.
- (iv) 6.552 MHz Filter and Gain - +/-364.5 KHz with 6 dB's gain.
- (v) QPSK Demodulator - Toshiba TA8662N.
- (vi) TI NICAM 728 Stereo Demultiplexer - CF70123
- (vii) Digital to Analogue Converters - I²S-Bus or S-BUS
compatible e.g. Philips SAA7220 & TDA1541 or ITT APU2470

3. Architecture

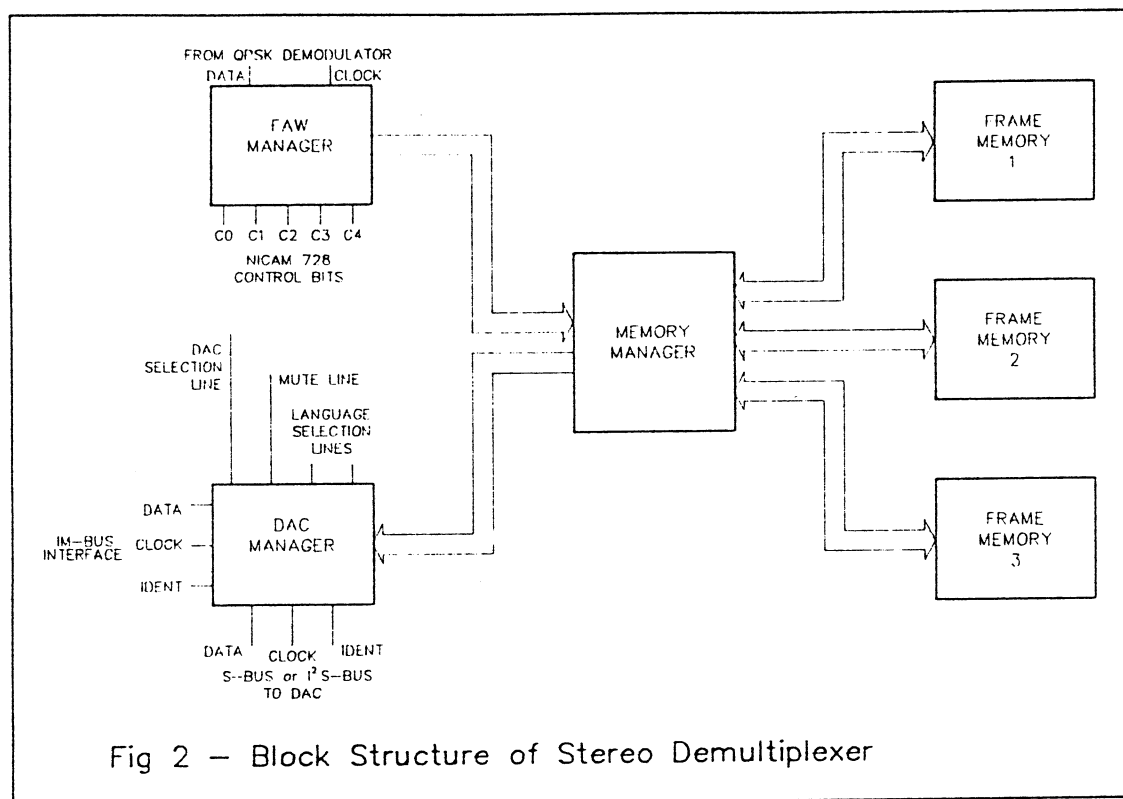


Fig 2 – Block Structure of Stereo Demultiplexer

Frame Alignment Word (FAW) Manager

This block accepts the serial 728 kbit/s data stream from the QSPK demodulator and using the FAW, locks onto the data stream. The data stream is then de-scrambled before being passed to the memory manager.

Memory Manager

This block accepts descrambled sound samples from the FAW manager, de-interleaves and writes them into one of the three frame memories. The memories are organised as 64 X 11 bits and therefore each can hold one frame of sound samples. The Memory Manager also allows for reading of the stored samples when required by the DAC Manager.

Because the samples are interleaved it is necessary to have more than one frame memory, such that whilst the current frame is being de-interleaved, the previous frame is being output. However, because of the format used for dual language transmissions, to achieve simultaneous output of both languages, three frame memories are required.

DAC Manager

This block firstly reads the appropriate frame memory via the memory manager. From these companded samples the range information is extracted, and the 14-bit samples recovered. The original parity is now reconstituted, and error checking and recovery is performed using the parity information and the protection ranges. The samples are then output to the digital to analogue converters using the appropriate bus format.

**SINGLE CHIP NICAM 728
STEREO DEMULTIPLEXER
CF70123**

Table 1 - Pin Description of Stereo Demultiplexer

4. Pin Description

SIGNAL	PIN	I/O	TYPE (*)	DESCRIPTION
Vcc	1			POWER SUPPLIES PWR Supply Voltage (+5V Nom.) Both pins must be connected. However the same supply can be used for both pins.
	21			
GND	10 13 27 30			All four pins must be connected to the digital ground of your system.
DACOSVC	9	O	C	CLOCKS DACOSC varicap drive. DACOSC output. DACOSC input, 16.384 Mhz required. SYSCLK input, 5.824 Mhz required. Selects whether varicap drive is required. Varicap drive for SYSCLK if required.
DACOSCOUT	11	O		
DACOSCIN	12	I		
SYSCLKIN	28	I	TS	
SYSCLKSEL	29	I	C	
SYSCLKVC	31	O	C	
DACCLKOUT	40	O	C	8.192/16.384 MHz clock output.
IMDAT	14	I/O	I=T O=C	INTERMETALL BUS INTERFACE I.M. Bus Data
IMDT	16	I	TS	
IMCLK	17	I	TS	
S/IDAT	3	O	C	S-BUS/I2S-BUS INTERFACE S/I2S-Bus Data S/I2S-Bus Clock S/I2S-Bus Ident
S/ICLK	4	O	C	
S/IIDT	33	O	C	
RESOUT	2	O	C	FLAGS Follows EXTRES input. Could be used as a reset signal for DAC's. Goes high while Auxiliary Data is being output on 728DAT. Goes high when a bad sample is being output on the S-Bus. (Still functional with I2S-bus, but is not in sync). Goes high while Frame Alignment Word and control bits are being output on 728DAT. Goes high to indicate that the demultiplexer has muted and is not outputting samples. These pins show the state of the NICAM 728 control bits arrived at by majority decision. Could be used for Stereo, Dual Language, Mono indicators with appropriate gating and buffering.
ADW	6	O	C	
ERRFLG	8	O	C	
FAACW	32	O	C	
MUTE	34	O	C	
C4	35	O	C	
C3	36	O	C	
C2	37	O	C	
C1	38	O	C	
C0	39	O	C	
DACSEL	18	I	C	CONTROL If held high, I2S-Bus is selected.(Phillips DAC's). If held low S-Bus is selected.(ITT DAC's). This is for test purposes, allowing the demultiplexer to process test transmissions. This is for test purposes, allowing the mute feature of the demultiplexer to be disabled. Selects language for DACS 1 & 2. Selects language for DACS 3 & 4. This is used to reset the device. Active low.
C4EN	19	I	C	
MUTEEN	20	I	C	
DACS1+2	24	I	C	
DACS3+4	25	I	C	
EXTRES	26	I	TS	
728CLK	5	O	C	NICAM SIGNAL PATH 728 KHz clock synchronized to 728DAT. Output of complete NICAM 728 data stream after descrambling. Accepts a descrambled NICAM 728 data stream. 728 KHz clock input from QPSK demodulator. 728 Kbit/s NICAM 728 data stream input from QPSK.
728DAT	7	O	C	
EXTDAT	15	I	C	
QPSKCLK	22	I	TS	
QPSKDAT	23	I	TS	

(*) C=CMOS T=TTL TS=TTL Schmitt

5. Device Initialisation

Initialization of the demultiplexer can be effected by taking EXTRES(Pin 26) low. On power-up, the demultiplexer automatically resets. External components are not required to achieve this.

An output RESOUT(Pin 2) is provided, which follows EXTRES. RESOUT also goes low during a power-up reset. This could be used as a reset signal for the Digital-to-Analogue converters

Refer to Electrical Specifications for reset timing.

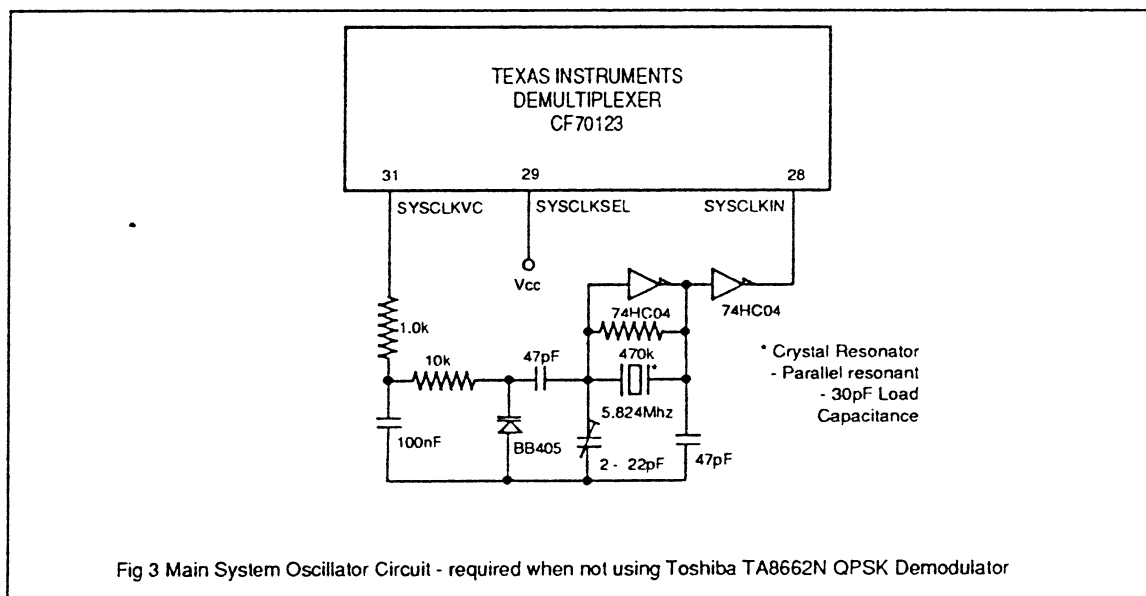
6. Oscillators

The demultiplexer requires two clock inputs, SYSCLK which is the main system clock, and DACOSC which sets the data rate for the output to the digital to analogue converters.

a) SYSCLK - An oscillator of 5.824 MHz is required. This can be implemented by two methods :-

Method 1 The Toshiba TA8662N QPSK demodulator has a 5.824 MHz clock output, and this can be used to implement SYSCLK, by connecting directly to pin 28, SYSCLKIN.

Method 2 If you are using a QPSK demodulator without a 5.824 MHz output, then the circuit of figure 3 is required



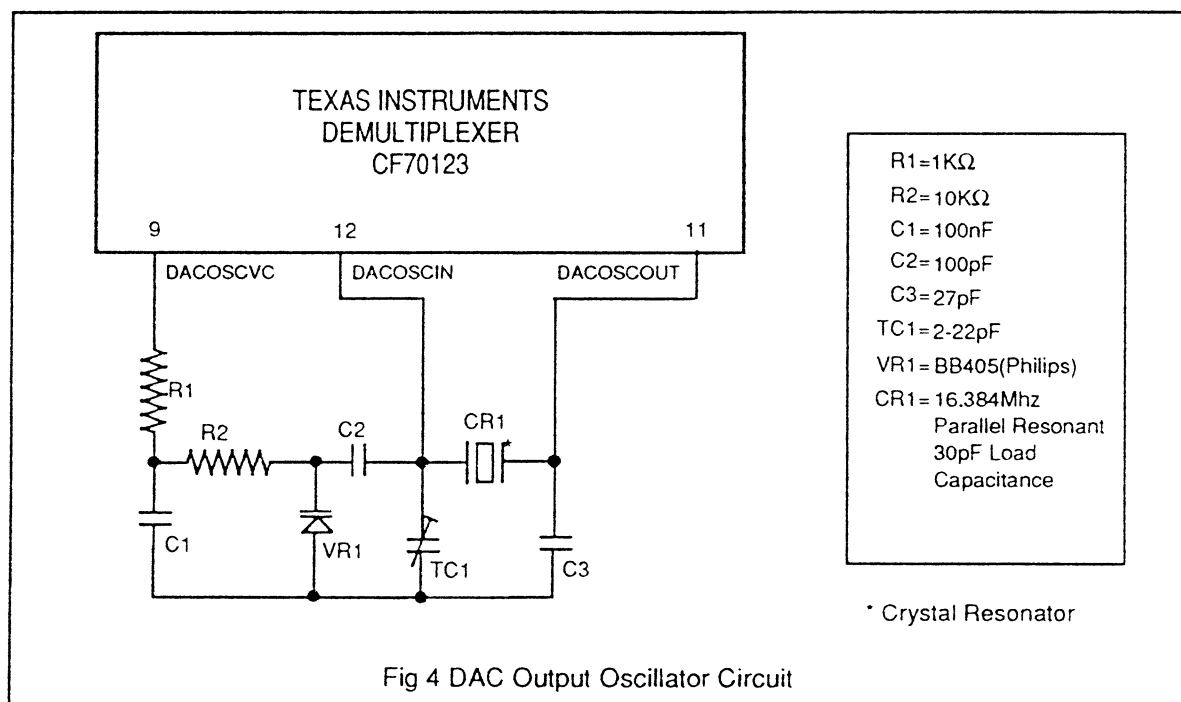
Pin 29, SYSCLKSEL is used to select which method is being used.

LEVEL '0' Selects QPSK derived clock	-Method 1
LEVEL '1' Selects circuit of figure 3	-Method 2.

6.Oscillators - continued

b) DACOSC

The frequency required is 16.384 MHz. The circuitry of figure 4 is required to implement this oscillator -



Pin 40, DACCLKOUT provides a clock signal that can be used to clock your D/A converters. The frequency of this clock is dependent on the state of DACSEL, Pin 18 :

- a) DACSEL = Logic '0' DACCLKOUT = 16.384 Mhz
- b) DACSEL = Logic '1' DACCLKOUT = 8.192 Mhz

7. Input from the QPSK demodulator

Two signals are required from the QPSK demodulator as input to the demultiplexer: a 728 Kbits/s NICAM 728 encoded digital data stream and an associated 728 KHz clock, the data stream being clocked by the positive going edge of the clock signal. The relationship between the two signals is shown in Figure 5.

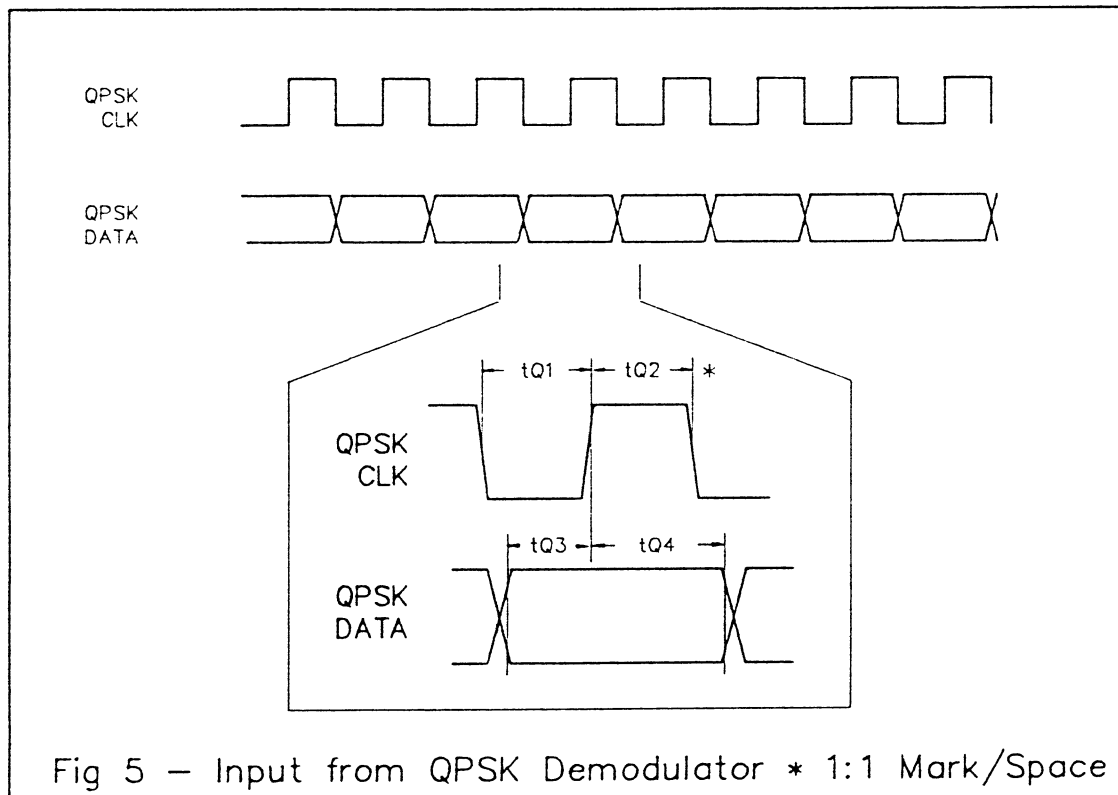


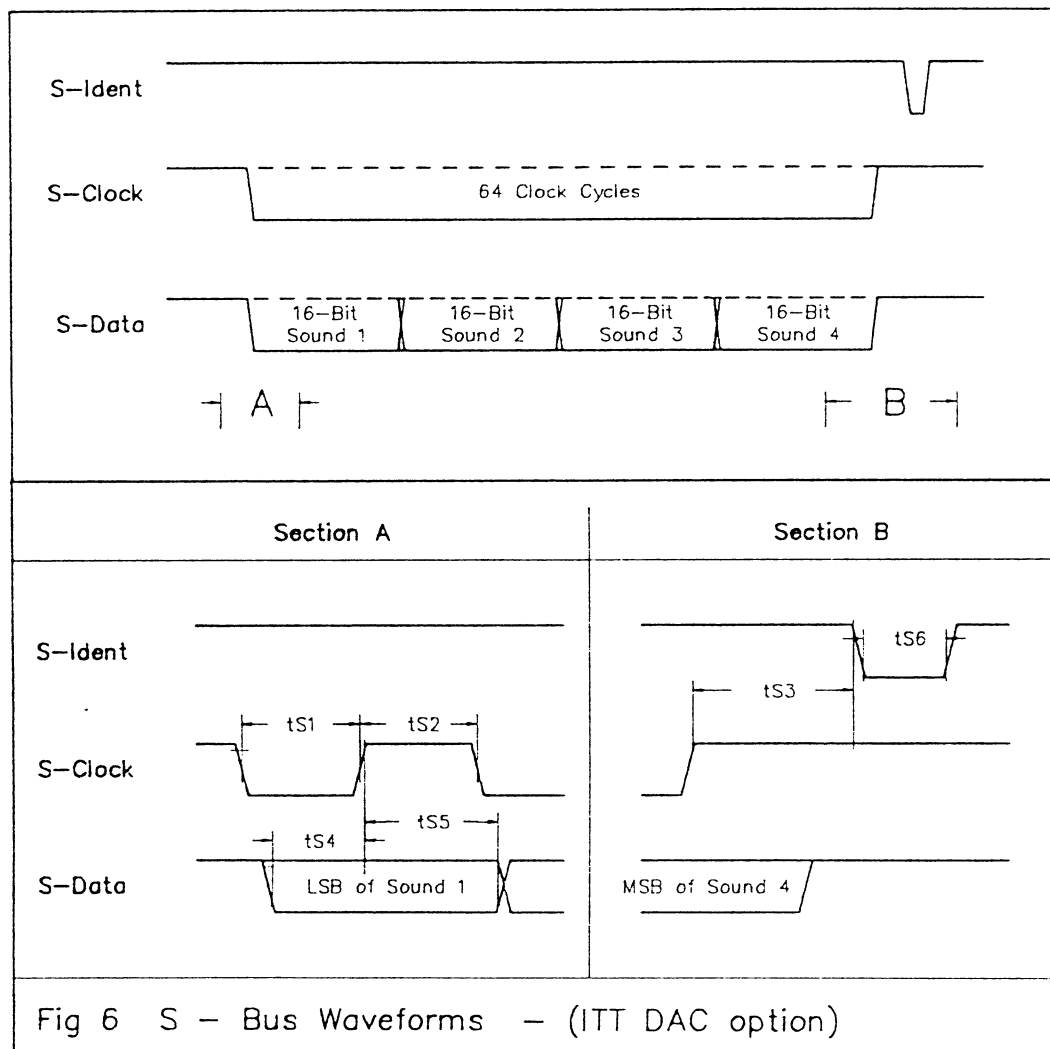
Fig 5 — Input from QPSK Demodulator * 1:1 Mark/Space

8.Interface to digital to analogue converters

The demultiplexer can be used with digital to analogue converters that are compatible with I²S-BUS or S-BUS formats e.g. Philips SAA7220 & TDA 1541 and ITT APU2470. The format required is selected by a single pin (DACSEL, pin 18) : Logic '1' indicates I²S-Bus, Logic '0' indicates S-BUS. Also, by using some simple interface circuitry, it is possible to use Toshiba DAC's. This is detailed in Appendix 1.

The Philips SAA7220 oversampling filter has the capability to interpolate in the case of an erroneous sample. Hence, ERRFLG is provided on the demultiplexer to flag erroneous samples to the filter (See Fig 7).

Figure 6 and Figure 7 show the formats of the S-Bus and I²S-BUS respectively.



8.Interface to digital to analogue converters - continued

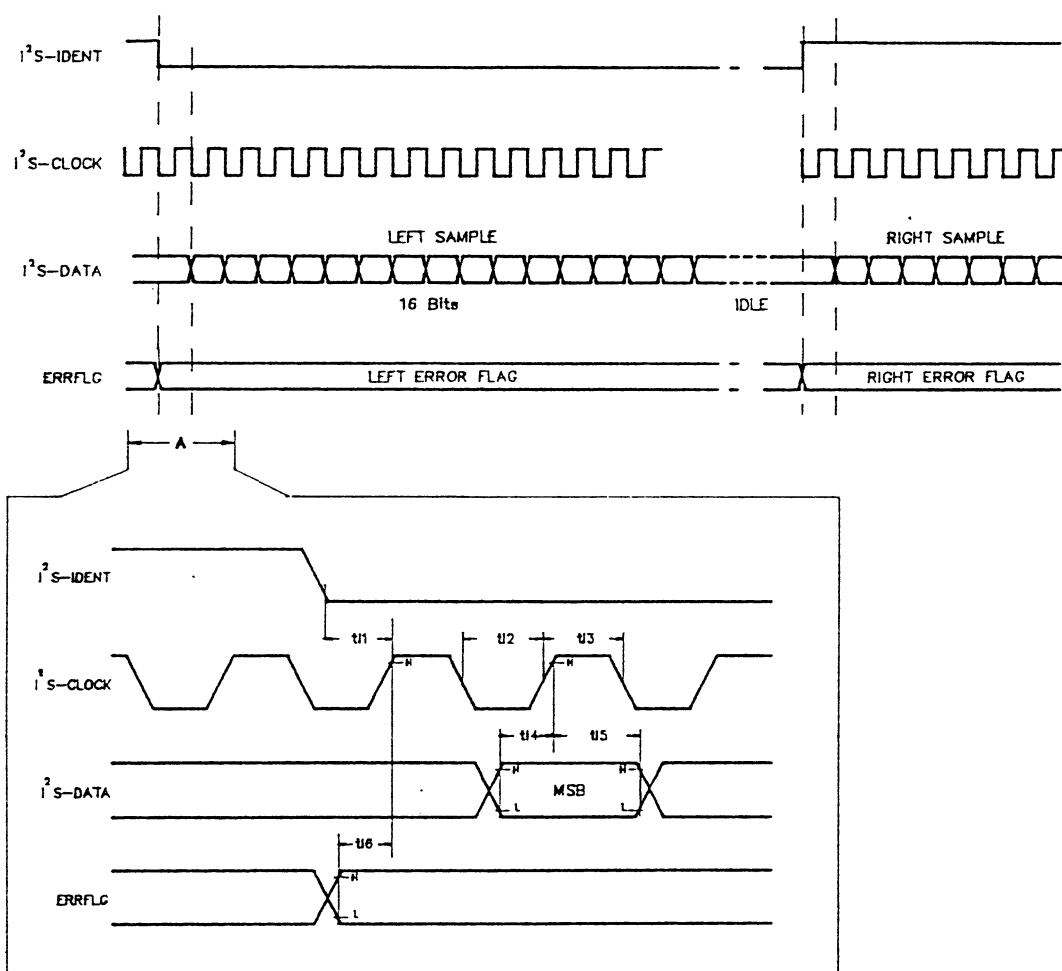


FIG 7 I²S-Bus Waveforms (plus ERRFLG)

9. Connection of demultiplexer into your system

The demultiplexer has been designed for ease of use in most TV systems. The device can be controlled, and information obtained from it by two methods. The first method is by using the external pins, the second is to use the IM-Bus interface.

Using either method it is possible to do the following:-

- (i) Determine the state of the NICAM control bits;
- (ii) Determine whether the demultiplexer has muted;
- (iii) Select language during dual language transmissions.

1. Using External Pins

a) Pins C0,C1,C2,C3,C4 - These indicate the state of the NICAM control bits (a description follows). They could be used to drive front panel indicator lights via appropriate gating and buffering.

C0 - The Frame Flag Bit

This is set to logic '1' for 8 successive frames and to '0' for the next 8 frames; thus defining a 16 frame sequence. The first frame of the sequence is defined to be the first of the frames in which C0 = Logic '1'. This frame sequence is used to synchronise changes in the type of information being broadcast.

C1,C2,C3 - The Application Control Bits

These three bits indicate the type of information being broadcast. Table 2 indicates the available options

These control bits can only change to indicate a new type of information on Frame 1 of the 16-frame sequence. The actual information type will then change on Frame 1 of the following 16-frame sequence.

Table 2 - Application Control Bits

C1	C2	C3	TYPE
0	0	0	Stereo signal comprising alternate A & B channel samples
0	1	0	Two independent mono sound signals transmitted in alternate frames (Dual Language)
1	0	0	One mono signal and one 352 kbits/s data channel transmitted in alternate frames
1	1	0	One 704 kbit/s data channel.

C4 - The Reserve Sound Switching Flag

This bit is set to logic '1' to indicate that the FM mono signal is carrying the same sound programme as the digital stereo signal. In the case of dual language transmissions, a logic '1' indicates that language 1 is the same as the FM mono signal.

b) MUTE Pin - When pin MUTE is logic '1' it indicates that the demultiplexer has muted and is not outputting samples.

9.Connection of demultiplexer Into your system - continued

c) Pins DACS1+2 & DACS3+4 - Allow selection of language during dual language transmissions.
Table3 indicates the options available :-

Table 3 - Language Selection

PIN		ITT/ PHILIPS DAC	DACS 1 & 2		DACS 3 & 4	
DACS 1+2	DACS3+4		LEFT(1)	RIGHT(2)	LEFT(3)	RIGHT(4)
0	0	PHILIPS	L1	L1	N/A	N/A
0	1	PHILIPS	L1	L2	N/A	N/A
1	0	PHILIPS	L2	L1	N/A	N/A
1	1	PHILIPS	L2	L2	N/A	N/A
0	0	ITT	L1	L1	L1	L1
0	1	ITT	L1	L1	L2	L2
1	0	ITT	L2	L2	L1	L1
1	1	ITT	L2	L2	L2	L2

L1 = Language 1 L2 = Language 2 N/A = Not Available

Pins DACS1+2 and DACS3+4 only have any effect when the control bits are indicating dual language format. In stereo format, the sound is routed to both DACS 1 & 2 and DACS 3 & 4. In mono+data format, the mono sound is routed to DACS 1,2,3 & 4.

The DAC Numbers 1 - 4, indicate to which DAC on the ITT APU2470 the language is being routed. For the Philips DAC, Numbers 1 and 2 only apply.

9.Connection of demultiplexer into your system - continued

2. Using the IM-Bus Interface

The demultiplexer has two IM-BUS addresses associated with it, address 242 (Binary 11110010) is for reading, and address 243 (Binary 11110011) is for writing. The formats for reading and writing data are shown below.

Reading	LSB	C1	Status of Control Bit 1.
		C2	Status of Control Bit 2.
		C3	Status of Control Bit 3.
		C4	Status of Control Bit 4.
		MUTE	Logic '1' indicates Stereo Broadcast Failed.
		DACS1+2 DACS3+4	These bits indicate the language selected and are valid during dual language format only - please refer to * below.
	MSB	BLANK	Logic '0'
Writing	LSB	BLANK	Set to Logic '0'.
		DACS3+4 DACS1+2	These bits allow for the selection of language and have effect only during dual language format - please refer to * below.
		IMEN	Logic '1' Enables IM-Bus control.
		HIZSBUS	Sets S-Bus outputs to high impedance.
		BLANK	Set to Logic '0'.
		BLANK	Set to Logic '0'.
	MSB	BLANK	Set to Logic '0'.

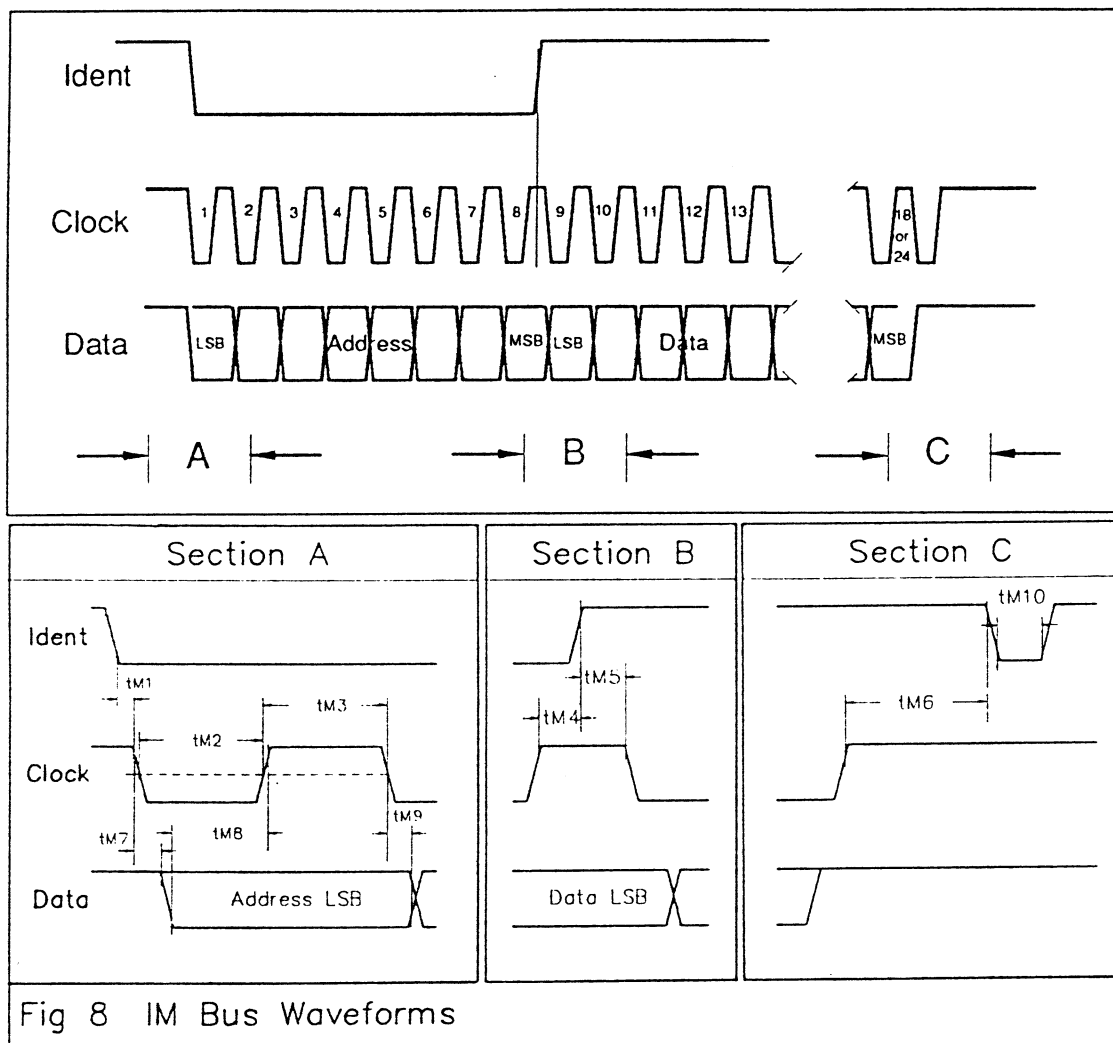
* When using bits DACS1+2 and DACS3+4 these can be viewed as though they are the external pins DACS1+2 and DACS3+4. Table 3 then applies in the same manner.

Setting HIZSBUS to Logic '1' sets the DAC output bus (S-BUS or I²S-BUS) to a high impedance state.

To allow control of the demultiplexer via the IM-BUS, please note that the IMEN bit must be set to logic '1'

Figure 8 opposite shows the format for the data transfer on the IM-BUS.

Please note that the IMDAT(Pin 14) is in fact a pseudo open-drain when in output mode. As such it requires an external 2.5k pull-up resistor for correct operation. However, when using ITT CCU's, the pull-up resistor is not required as it is incorporated in the CCU.



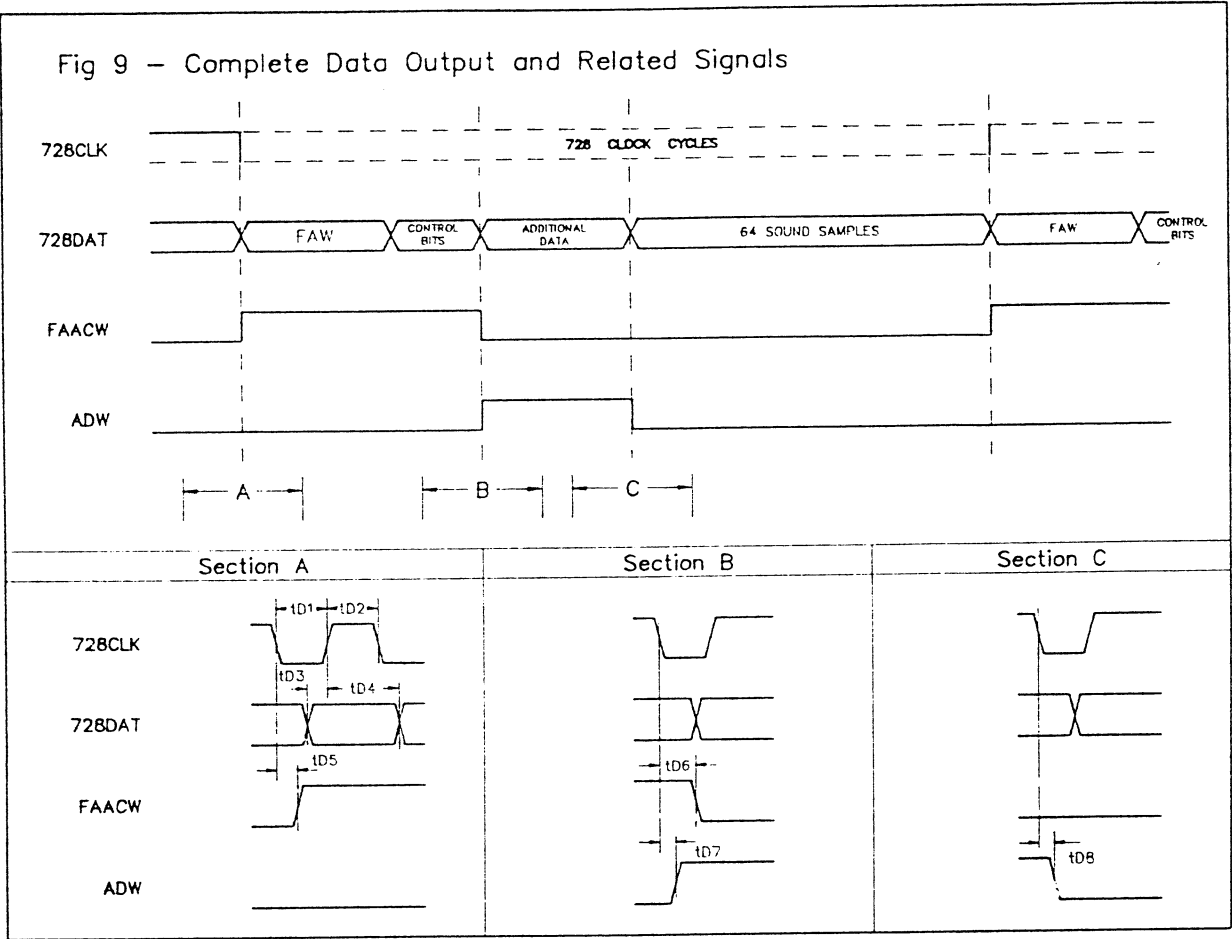
10. Addition of external pseudo random sequence generator

Although the demultiplexer descrambles the incoming data stream, it is possible that extra scrambling could be added before transmission - for secure transmission applications. To allow the demultiplexer to process this mode of transmission, the complete NICAM 728 data stream is brought off chip after it has been through the normal NICAM descrambling. This is done via 728DAT(Pin 7). This pin has an associated clock signal - 728CLK(Pin 5).

If extra descrambling is not required, then 728DAT is simply routed back on chip via EXTDAT(Pin 15). If extra descrambling is required then extra circuitry must be added between 728DAT and EXTDAT to do this. When adding circuitry please note that the data cannot be latched between 728DAT and EXTDAT. Only one gate delay can be tolerated (This would be an Exclusive-OR gate when adding a Pseudo Random Sequence Generator) - refer to electrical specifications for precise timing information.

To aid descrambling two window signals are provided. The first is a Frame Alignment Word and Control Bit Window (FAACW - Pin 32). This signal is at logic '1' while the frame alignment word and the control bits are being output via 728DAT. The second is an Additional Data Window. This is logic '1' while the additional data bits are being output.

The relationship between all the relevant signals is shown in Fig 9 overleaf.



11. Testing facilities

Pins MUTEEN and C4EN are provided to allow system prototyping and testing.

Normally the demultiplexer will mute when greater than 1 in 100 parity errors are detected. It will unmute when less than 1 in 400 parity errors are detected. If you are trying to set up a system and the demultiplexer is muted, it may be difficult to establish if a fault exists. Thus if logic '1' is applied to MUTEEN the demultiplexer will not mute and will output all data irrespective of error rate.

11. Testing facilities - continued

In the NICAM 728 data stream, control bit 4 indicates whether the FM mono broadcast and the stereo broadcast are transmitting the same material. If this bit is logic '0', indicating the broadcasts are different, the demultiplexer will mute, thus allowing external circuitry to switch to the FM transmission. If logic '1' is applied to C4EN, this stops the demultiplexer muting under the above circumstances, allowing test transmissions to be processed.

The demultiplexer assumes that if the FM mono and stereo broadcasts are different, then the stereo transmission is a test transmission and is not required in normal domestic use. Table 4 summarises the state of the mute pin in relation to the transmitted control bit 4 and C4 enable, and also under weak and strong signal conditions.

Table 4. State of mute line with respect to C4EN

		Weak Stereo Transmission		Good Stereo Transmission	
Transmitted Control bit 4	C4EN	Preferred Transmission	Mute Line	Preferred Transmission	Mute Line
0	0	FM	1	FM	1
0	1	FM	1	STEREO	0
1	0	FM	1	STEREO	0
1	1	FM	1	STEREO	0

12. Use of the Demultiplexer in countries using the FULL EBU NICAM specification e.g. Nordic countries

In these countries, parity bits 55 to 64 are used to define two bits of binary control information (CIB). To allow for compatibility, the CF70123 decodes this information such that the original parity can be reconstituted. However, this information is not available externally. Hence, the CF70123 permits the CIB's to have a "Don't Care" value.

13.Applications diagrams

Fig 10 illustrates a simple system using I²S-BUS compatible DAC's and a Toshiba QPSK demodulator.

Fig 11 shows a more complex system using S-BUS compatible DAC's and a controlling microprocessor. Again a Toshiba QPSK demodulator is used.

Fig 12 shows a generalised system in which the 5.824 Mhz clock has been derived independently from the QPSK demodulator.

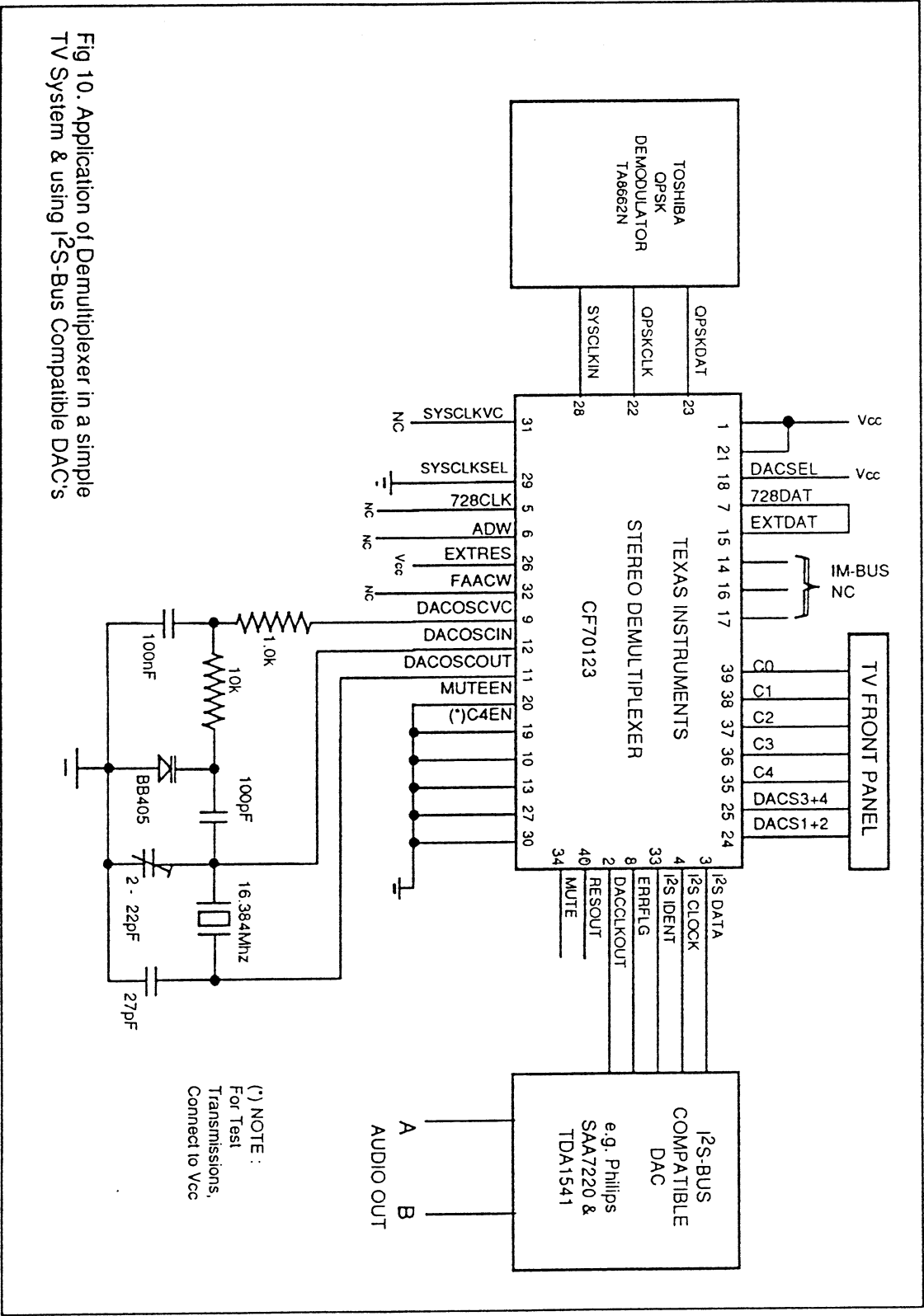
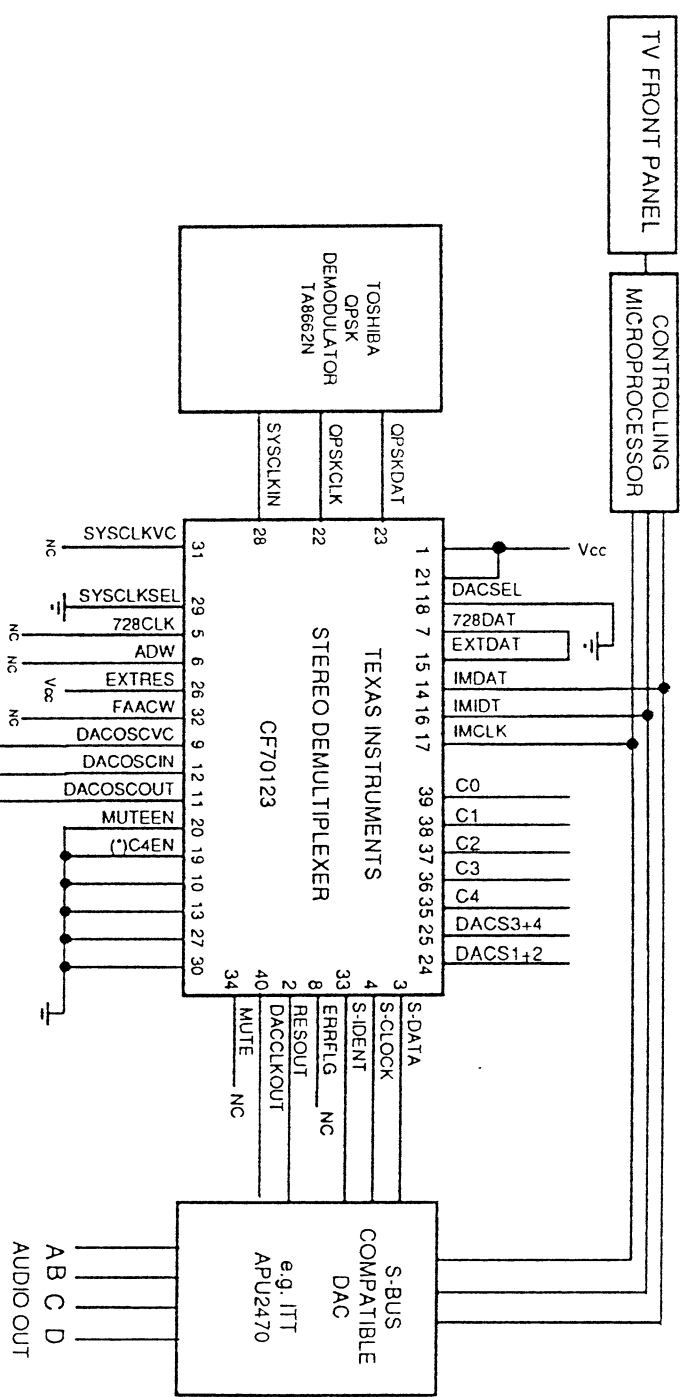
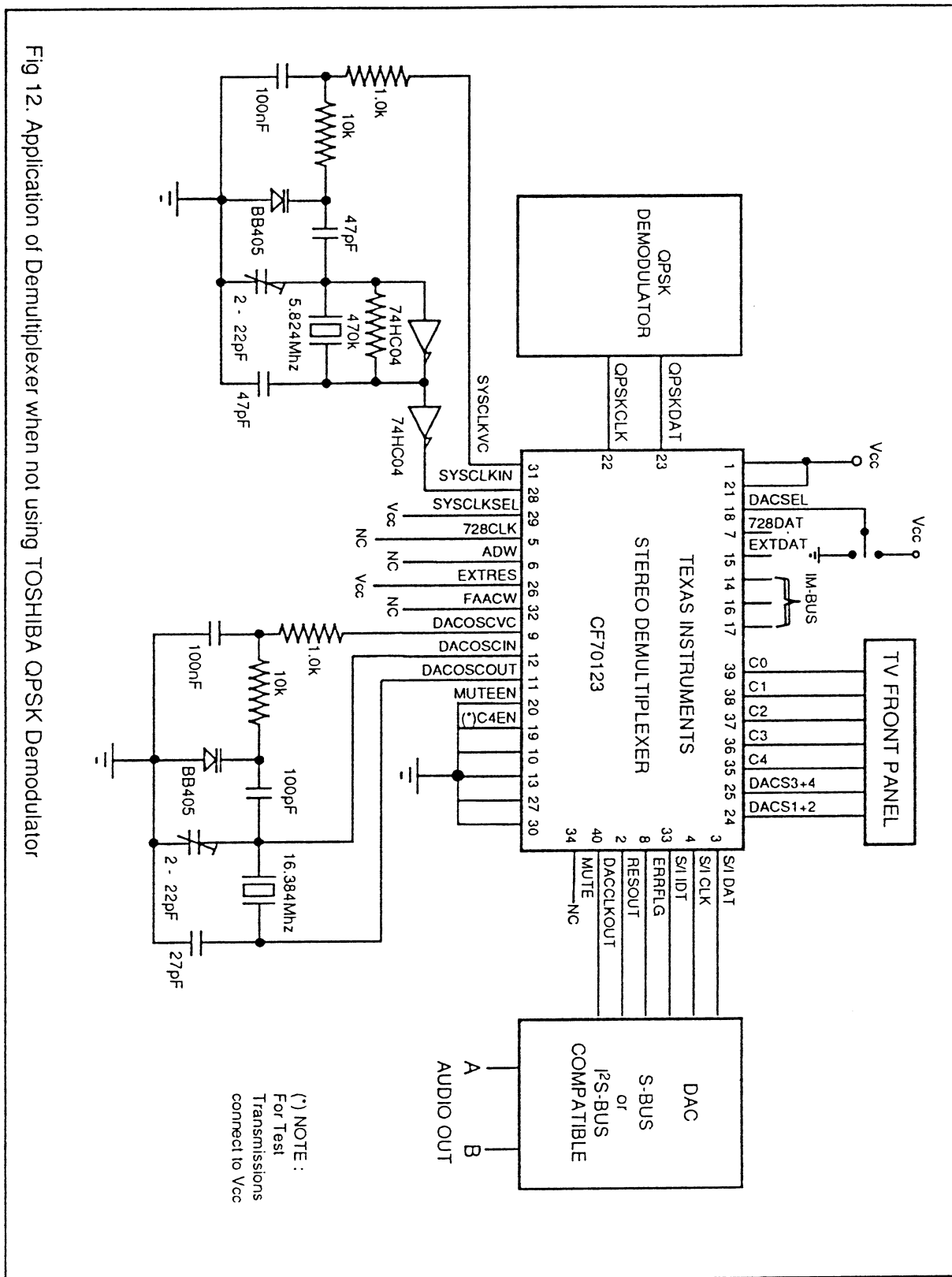


Fig 11. Application of Demultiplexer in a TV System
with a Microprocessor and using S-BUS Compatible
DACs



(*) NOTE :
For Test
Transmissions,
Connect to Vcc



14. PCB Layout Guidelines

When laying out a PCB for a NICAM 728 decoding system, it is advisable ensure minimum interaction between the different parts of the system (i.e. QPSK demodulator, stereo demultiplexer and DAC's). The following list of guidelines may be found useful :-

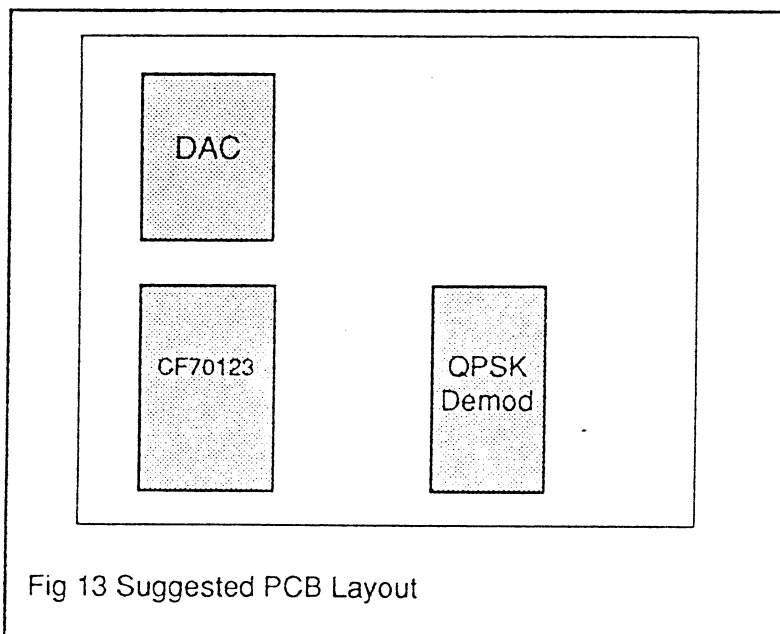
- (i) Have separate digital and analogue grounding, especially around the DAC's.
- (ii) Keep the grounding of different parts of the system as separate as possible.
- (iii) Use ground planes wherever possible.
- (iv) Lay out the PCB to keep radiation to a minimum. Incorrect layout of PCB's can cause problems with the following signals radiating to such an extent that the QPSK demodulator is affected and starts to produce erroneous data.

DACCLKOUT (Pin 40)
S/I IDT (Pin 33)
S/I DAT (Pin 3)
S/I CLK (Pin 4)

This is especially so when using the demultiplexer in the S-BUS mode. However, the problem can be cured by careful PCB layout - a satisfactory layout is shown in Fig 13.

The points to bear in mind are :-

- (i) Keep the connections of the above signals as short as possible.
- (ii) Keep the tracks for these signals away from the QPSK demodulator.



15. Electrical specifications

Absolute maximum ratings over operating free air temperature range

	Min	Nom	Max	UNIT
Supply Voltage V_{cc}			7	V
Input Voltage V_i			6	V
Input Diode Current I_{ik} ($-0.5V > V_i > V_{cc}+0.5V$)			+/-20	mA
Output Diode Current I_{ok} ($-0.5V > V_i > V_{cc}+0.5V$)			+/-20	mA
Continuous Current through V_{cc} & GND			+/-50	mA
Operating Free Air Temperature Range			0/70	°C
Lead Temperature 1.6mm from Case (Plastic)			260	°C
Storage Temperature			-65 to 150	°C

recommended operating conditions

Parameter	Description	Conditions	Min	Nom	Max	UNIT
V_{cc}	Operating Supply Voltage		4.5	5.0	5.5	V
T_{amb}	Operating Temp. Range		0		70	°C
I_{ih}	Input Leakage Current - High	$V_i = V_{cc}$ $V_{cc} = \text{Max}$ Inputs Bidirectionals DACOSCIN EXTRES $V_i = 4V$	2 55	115	+/-1 +/-11 +30 290	μA μA μA μA
I_{il}	Input Leakage Current - Low	$V_i = V_{ss}$ $V_{cc} = \text{Max}$ Inputs Bidirectionals DACOSCIN EXTRES $V_i = 4V$	-2 125	250	+/-1 +/-11 -30 625	μA μA μA μA
V_{ih}	Input High Threshold Voltage	$V_{cc} = \text{Min/Max}$ TTL CMOS (inc DACOSCIN)	2 0.7V $_{cc}$			V V
V_{il}	Input Low TTL CMOS (inc DACOSCIN)	$V_{cc} = \text{Min/Max}$			0.8 0.2V $_{cc}$	V V
$V_{t+} - V_{t-}$	Hysteresis on Schmitt trigger inputs		200			mV

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recommended operating conditions - continued

Parameter	Description	Conditions	Min	Nom	Max	UNIT
V _{oh}	Output Voltage High V _{cc} =Min Note : IMDAT (*)	I _{oh} =40uA	V _{cc} -100mV			V
		I _{oh} =400uA	V _{cc} -200mV			V
		I _{oh} =4mA	3.76			V
V _{oh}	DACOSCOU	V _{cc} =Min				
		I _{oh} =60uA	V _{cc} -100mV			V
		I _{oh} =600uA	V _{cc} -200mV			V
V _{ol}	Output Voltage Low	V _{cc} =Min I _{ol} =40uA I _{ol} =4mA			100	mV
					400	mV
I _{oz}	3-state Leakage Current Outputs only	V _{cc} =Max V _o =V _{cc} or V _{ss}			+/-10	uA
I _{ccq}	Static Current Outputs open Oscillator high & static RAM inactive	V _{cc} =Max,			1	nA
I _{cca}	RMS Average Current Outputs open. Integrated during test pattern execution	V _{cc} =Max,			50	mA

(*) NOTE : IMDAT is incapable of driving high on its own - it is a pseudo open-drain output

Timing requirements over recommended operating range

Parameter	Description	Min	Nom	Max	UNIT
t _{RES}	EXTRES input low time to ensure reset		100		ms
f _D	Frequency of 728CLK output		728		kHz
t _{D2} /t _{D1}	728CLK output high/low ratio		1		
t _{D3}	728DAT output setup time	650	675		ns
t _{D4}	728DAT output hold time	680	780		ns
DATDEL	Allowable delay between 728DAT and EXTDAT inputs			640	ns
t _{D5}	Delay time of rising edge of FAACW output after falling edge of 728CLK output	-15	2	15	ns

Timing requirements over recommended operating range - continued

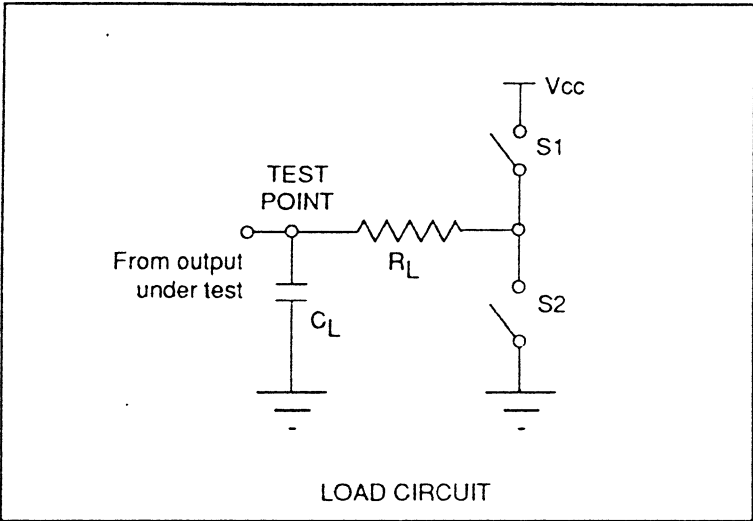
Parameter	Description	Min	Nom	Max	UNIT
tD6	Delay time of falling edge of FAACW output after falling edge of 728CLK output	-15	5	15	ns
tD7	Delay time of rising edge of ADW output after falling edge of 728CLK output	-15	3	15	ns
tD8	Delay time of falling edge of ADW output after falling edge of 728CLK output	-15	5	15	ns
tI1	I ² S-BUS IDENT output setup time before rising edge of CLOCK output	225	240		ns
tI3/tI2	I ² S-BUS. CLOCK output high/low ratio		1		
fI	Frequency of I ² S-BUS clock output		2.048		Mhz
tI4	I ² S-BUS DATA output setup time before rising edge of CLOCK output	200	225		ns
tI5	I ² S-BUS DATA output hold time after rising edge of CLOCK output	235	260		ns
tI6	ERRFLG setup time before rising edge of I ² S-BUS CLOCK output	235	245		ns
tM1	IM-BUS CLOCK input delay time after falling edge of IDENT input	0			ns
IMfreq	IM-BUS input clock frequency	0.05		170	kHz
tM2	IM-BUS CLOCK input low time	3.0			us
tM3	IM-BUS CLOCK input high time	3.0			us
tM4	IM-BUS CLOCK input setup time before IDENT input high	0			ns
tM5	IM-BUS CLOCK input hold time after IDENT input high	1.5			us
tM6	IM-BUS CLOCK input high time before IDENT END-PULSE input	6.0			us
tM7	IM-BUS DATA input delay time after falling edge of CLOCK input	0			ns
tM8	IM-BUS DATA input setup time before rising edge CLOCK input	0			ns

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Timing requirements over recommended operating range - continued

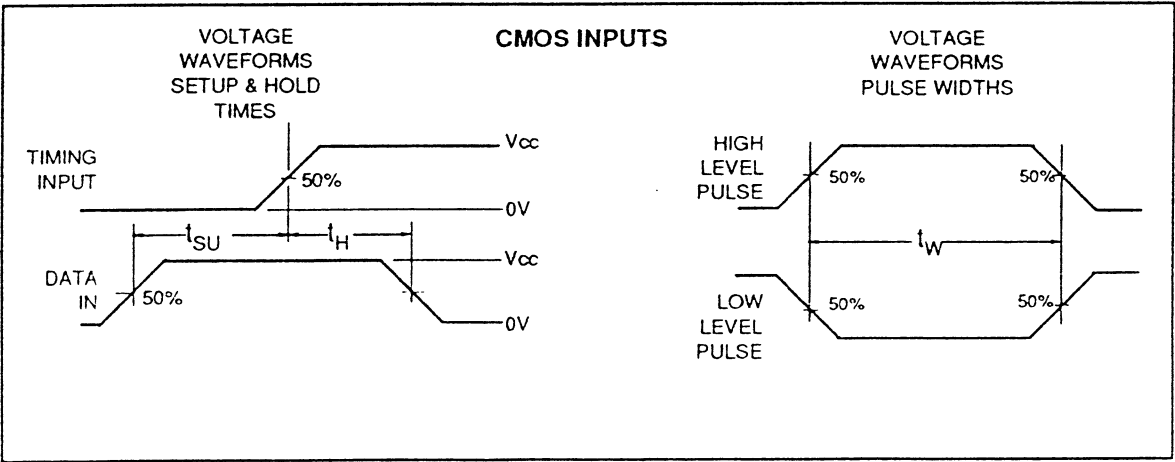
Parameter	Description	Min	Nom	Max	UNIT
tM9	IM-BUS DATA input hold time after falling edge of CLOCK input	0			ns
tM10	IM-BUS IDENT end-pulse low time	3			us
fS	Frequency of S-CLOCK output		4.096		Mhz
tS2/tS1	S-BUS CLOCK output high/low ratio				
tS3	S-BUS CLOCK output high time before IDENT end-pulse output	240	255		ns
tS4	S-BUS DATA output setup time before rising edge of CLOCK output	80	101		ns
tS5	S-BUS DATA output hold time after rising edge of CLOCK output	115	135		ns
tS6	S-BUS IDENT end-pulse output low time	225	240		ns
fQ	Frequency of QPSK clock input		728		kHz
tQ2/tQ1	QPSK clock input high/low ratio		1.0		
tQ3	QPSKDAT input setup time	10			ns
tQ4	QPSKDAT input hold time	60			ns

16.Parameter Measurement Information

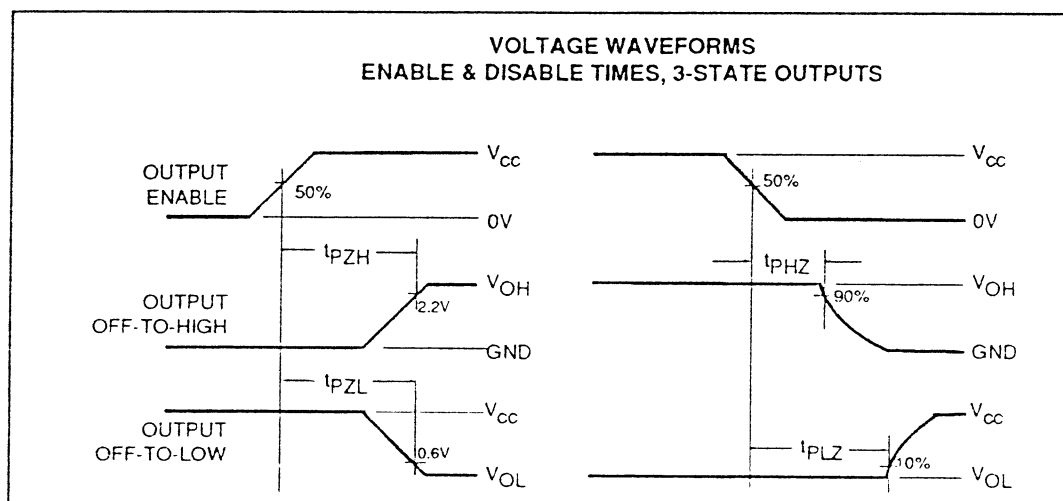
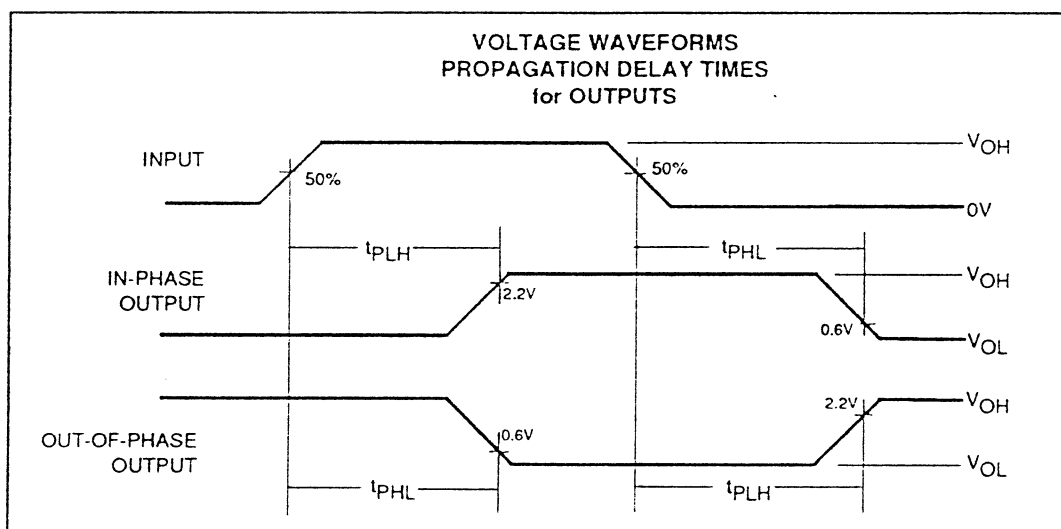
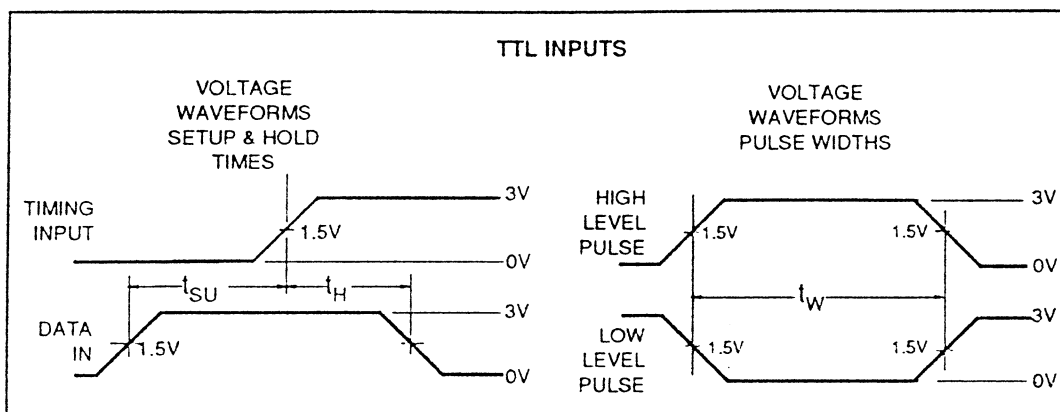


Parameters	Test Conditions			* R_L	* C_L	S1	S2
tPLH/tPHL	Vcc =Nom	Standard Outputs	Totem	Inf	50	Open	Open
		High Current Outputs	Totem	Inf	150	Open	Open
		Standard	O/C	1	50	Closed	Open
		Standard	I/O	Inf	50	Open	Open
tPZH	Vcc=Nom	Standard 3-state	Totem	1	50	Open	Closed
tPZL	Vcc=Nom	Standard 3-state	Totem	1	50	Closed	Open
tPHZ	Vcc=Nom	Standard 3-state	Totem	1	50	Open	Closed
tPLZ	Vcc=Nom	Standard 3-state	Totem	1	50	Closed	Open

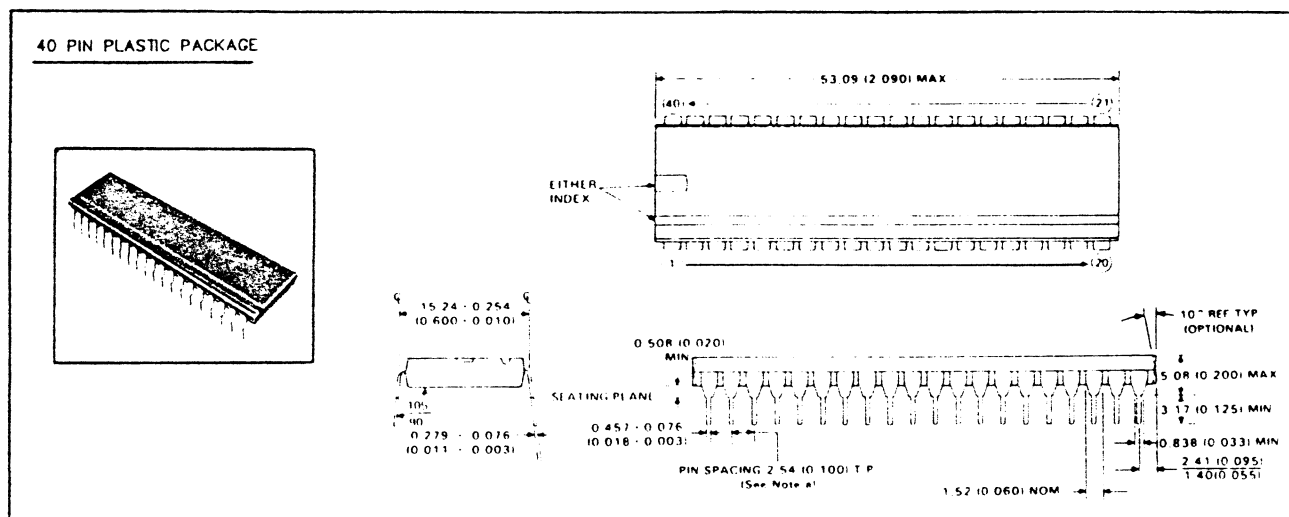
* R_L in $k\Omega$ * C_L in pF - includes test jig capacitance



16. Parameter Measurement Information - continued



17. Packaging Information



Note : Alternative packages may be made available subject to demand. Contact your local TI sales for further details.

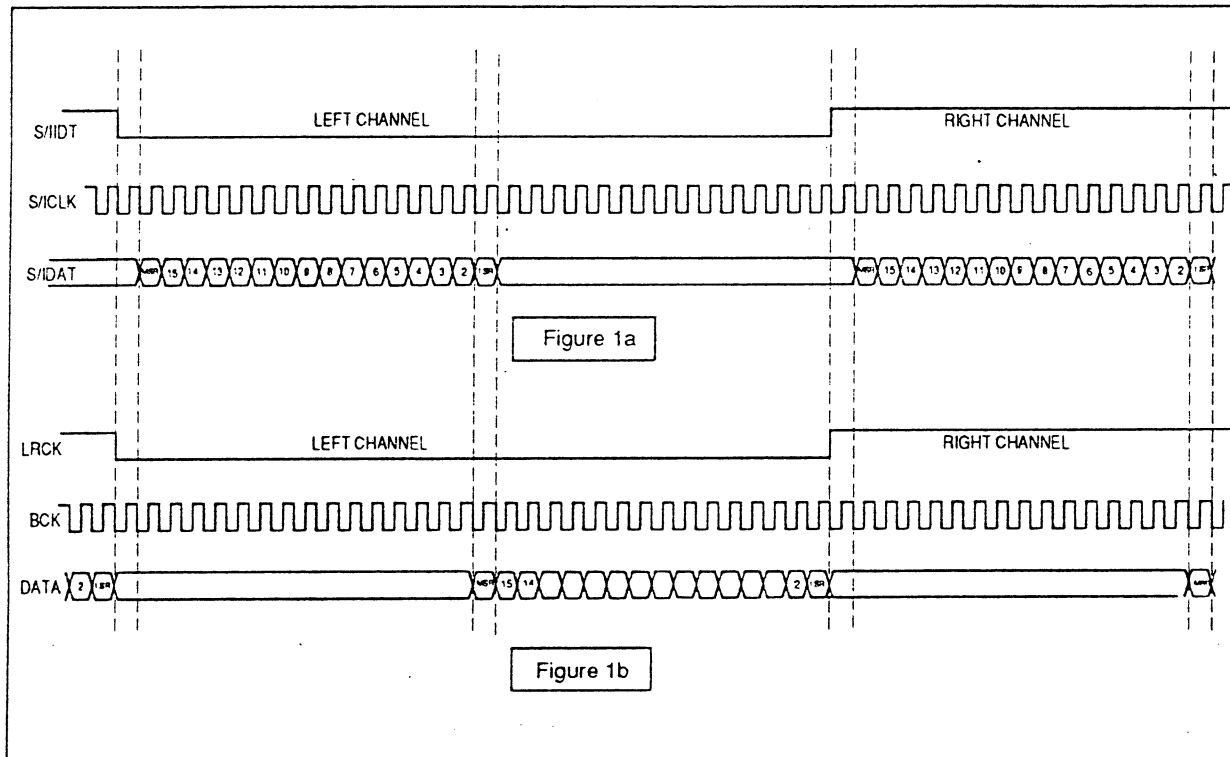
SINGLE CHIP NICAM 728
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APPENDIX 1

Introduction

The CF70123, although designed to work with Philips and ITT DAC's may also be used with Toshiba DAC's. This application brief describes the interface circuitry required.

The Interfacing problem



The input bus used with Toshiba's DAC's is, in fact, similar to the I²S-bus used by Philips DAC's. Figure 1a shows the I²S-bus produced by the CF70123. Figure 1b shows the bus format required by the Toshiba DAC's. Clearly, the only difference between these two formats is the position of the data bits in relation to the Ident lines (S/IIDT, LRCK).

Therefore, two solutions are possible :

- (i) - Delay the I²S-bus data line by 15 cycles of S/ICLK:
- (ii) - Delay the I²S-bus ident line by 17 cycles of S/ICLK. This now means that the ident line will be inverted with respect to the data, and so must be inverted.

Implementation of the Interface

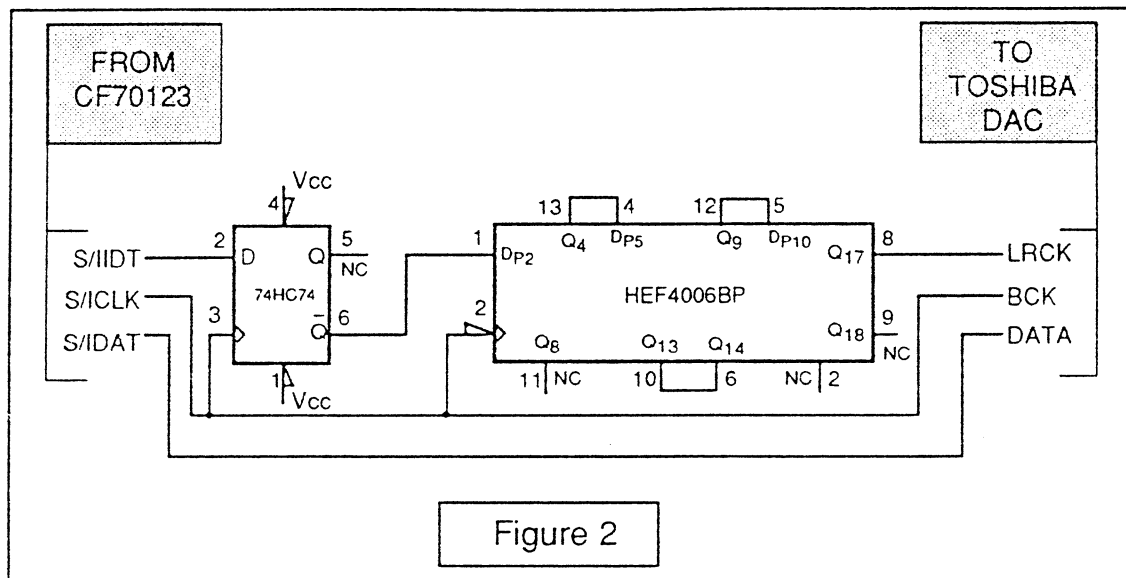


Figure 2 shows a satisfactory implementation of solution (ii). The HEF4006BP is an 18-bit shift register, but in this case, is wired as a 17-bit register. This gives the 17 cycle delay required in the I²S-bus Ident line. It is negative edge triggered, which means that the Ident line is correctly presented to the Toshiba DAC, changing on the negative edge of BCK (Figure 1b). However a latch is required in front of this register to accept the ident line on the rising edge of the clock and hold it for the HEF4006BP to accept on the next negative clock edge. By using the Q-bar output of the latch, the required inversion of the ident line is performed.

In order for this interface to work correctly at a data rate of 2.048 Mbits/s, it is essential that the shift register has a maximum propagation delay of less than 240ns. For this reason, it is recommended that a Signetics/Mullard HEF4006BP be used.

Conclusion

Interface of the CF70123 to Toshiba type DAC's and other DAC's using the same bus format is achievable at a low cost using the components described.